REMARKS/ARGUMENTS

Applicant has received the Office action dated April 28, 2005, in which the Examiner: 1) rejected claims 1, 12, 19 and 29 under 35 U.S.C. § 112, 2nd paragraph, as being indefinite; 2) rejected claims 12-28 under 35 U.S.C. § 102(e) as being anticipated by Trainin et al. (U.S. Pub. No. 2002/0144073); and 3) rejected claims 1, 3-11, 29-30 and 32-38 under 35 U.S.C. § 103(a) as being unpatentable over Trainin et al. in view of Steele, Jr. et al. (U.S. Pub. No. 2001/0056420).

With this Response, Applicant adds claim 39. Reconsideration is respectfully requested.

I. ARGUMENT

A. Section 112 Rejections

The Office action dated April 28, 2004 alleges that each of the independent claims suffer under Section 112, second paragraph, which Applicant respectfully traverses. In particular, the Office action states:

> It is not clear how software can perform memory operations without involving any hardware and it is not clear how hardware can perform the return of memory blocks without involving the use of software.

(Office action dated April 28, 2005). It is noted that none of the claims require that software perform any operation without hardware, or vice versa. While Applicant acknowledges that the Office uses the broadest reasonable interpretation in examining claims, Applicant submits that the interpretation is unreasonable, especially in view of the fact the Applicant is allowed to be his own lexicographer. With regard to "hardware device," the specification clearly states:

> A non-limiting list of hardware devices that could implement the heap memory management method comprises graphics cards, network interface cards, audio devices, and mass storage such as hard drives and compact disc drives.

(Specification Paragraph [0047]). Thus, Applicant respectfully submits that the interpretation of "software" and "hardware devices" in the Office action dated April 28, 2005 is not a reasonable interpretation in view of the subject matter of the specification. The reasonable interpretation that software does indeed

execute on hardware, and that the claimed hardware devices are devices such as such as graphics cards, network interface cards, audio devices, and mass storage devices moots the Section 112, second paragraph rejections.[1]

II. ART-BASED REJECTIONS

The Office action dated April 28, 2005 rejects the claims as allegedly anticipated by Trainin, or allegedly obvious over Trainin in view of Steele. Applicant respectfully traverses these rejections.

In accordance with embodiments of the invention, to implement concurrent non-blocking removal and returning of blocks of heap memory to a first end of the list by software streams requires atomic operations to the Top register 56, such as by using atomic compare-and-swap primitives. (Specification Paragraph [0039]). As the Examiner is no doubt aware, hardware devices such as graphics cards, network interface cards, audio devices, and mass storage devices are not part of the cache coherency domain of the main processor, and thus cannot perform atomic operations. The illustrative linked list of the current specification allows software streams to perform atomic operations on a first end of the linked list, and a hardware device can return memory blocks to the second end of the linked list in spite of the fact the hardware device is not capable of performing, or is not allowed to perform, atomic operations in a cache coherency domain to which it does not belong. The point being that neither Trainin considered alone, nor Trainin and Steele, enable a system as defined by the claims.

Trainin is directed to a method for memory heap management and buddy system management for service aware networks. (Trainin Title.) While Trainin may disclose free memory block management by way of a linked list (*See, e.g.*, Trainin Paragraph [0036]), Trainin makes no distinction between return of free memory blocks as between a software stream and a hardware device. Steele is directed to a lock-free implementation of a concurrent shared object with dynamic node allocation and a distinguishing pointer value. (Steele Title.) The Steele reference appears to be concerned only with concurrency between software

[1] And, for that matter, also distinguishes Trainin alone and Trainin in view of Steele.

streams executing within the same cache coherency domain, and thus does not even contemplate issues addressed by the current specification.

Claim 1, by contrast, specifically recites, "performing, **by a software stream**, heap memory operations on a first end of a linked list of free heap memory of a heap pile; and concurrently returning a return block of heap memory, **by a hardware device that used the return block of heap memory**, to the heap pile at a second end of the linked list of free heap memory." Applicant respectfully submits that Trainin taken with Steele fail to teach or fairly suggest that a hardware device[2] could or should return a block of heap memory concurrently with operations of a software stream. For these reasons, Applicants respectfully submit that claim 1 is not rendered unpatentable by Trainin and Steele, and that claim 1 should be allowed together with all claims that depend from claim 1 (claims 3-11).

Claim 12 specifically recites, "maintaining unused blocks of heap memory as a linked list, and wherein the unused blocks of the linked list comprise a first block at a beginning of the linked list, a second block pointed to the first block, and a third block at an end of the linked list; **removing, by a software stream, the first block from the linked list**, thus making the second block the beginning of the linked list; and **returning a return block, by a hardware device that used the return block, to the linked list by placing the return block at the end of the linked list.**" Applicant respectfully submits that Trainin fails to teach or fairly suggest that a hardware device could or should return a block of heap memory to a linked list that is also accessible by a software stream. For these reasons, Applicants respectfully submit that claim 12 is not rendered unpatentable by Trainin, and that claim 12 should be allowed together with all claims that depend from claim 12 (claims 13-18).

Claim 29 specifically recites, "a microprocessor executing a software stream; ... a first bridge logic device coupling the microprocessor to the main

[2] Reasonably construed in light of the specification to be devices, for example, graphics cards, network interface cards, audio devices, and mass storage devices.

memory array; a hardware device coupled to the heap memory through the first bridge logic device; wherein the software stream executed on the microprocessor removes blocks of heap memory from a beginning of the heap pile; and simultaneously the hardware device returns blocks of heap memory used by the hardware device to an end of the heap pile." Applicant respectfully submits that Trainin taken with Steele fail to teach or fairly suggest that a hardware device[3] could or should return a block of heap memory simultaneously with operations of a software stream. For these reasons, Applicants respectfully submit that claim 29 is not rendered unpatentable by Trainin and Steele, and that claim 29 should be allowed together with all claims that depend from claim 29 (claims 30 and32-38).

III. NEW CLAIM

With this Response, Applicant presents new claim 39. Applicant respectfully submits that neither Trainin nor Steele, alone or considered together, teach or render obvious the limitations of claim 39.

IV. CONCLUSION

In the course of the foregoing discussions, Applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of

[3] Which is clearly more than just "buses and registers" as construed in the Office action dated April 28, 2005 (page 13, third full paragraph), as the hardware device as claimed uses the heap memory.

time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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